BROADCOM®

Software Specification

35AT-4B Series

Battery Backup Multi-Turn RS485 Absolute Encoder

Description and General Specification

This document provides an explanation of the RS485 software specification for the 35AT series encoders.

Table 1 General Specification of the RS485 Serial Communication

Item	Specification	Note
Transmission Type	RS485 Compliant Differential Transceiver	
Communication Type	Half duplex	Recommended Transceiver: ISL8485E
Transmission Code Type	Binary, Non Return Zero (NRZ) code	
Synchronization Type	Asynchronous	
Communication Baud Rate	2.5Mbps	
Frame Length	10 bits/Frame	
Transmission Error Checking	8 bits CRC	CRC equation $G(X) = X^8 + 1$ X = cr0 ~ cr7

Definition of Encoder Operating Mode

Mode	Definition	VCC (Typ)	BATPWR (Typ)	Remarks
Power off mode	This is non-operation state of the encoder, where the main power supply, Vcc line and battery backup supply are not connected.	0V	0V	Before installation
Normal mode	This is normal operation state of the encoder, when main power supply Vcc is available. At this state, counting of single turn position, counting of multi-turn position and data transmission between encoder and Master are possible.	5V	3.6V	
Battery mode	This is battery backup operation stage, where the encoder is powered up by the backup battery connected to BATPWR input. At this state, only multi-turn counting is available.	0V	3.6V	

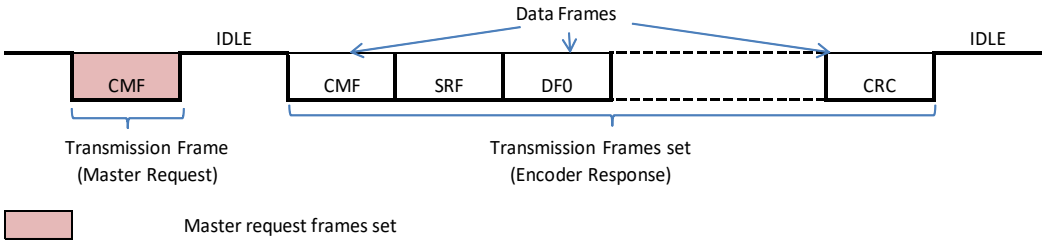
Table 2 Definition of Encoder Operating Mode

Transmission Frames between Master and Encoder

Overview of Communications

A one-to-one half-duplex serial communication is established between the encoder and the Master (e.g. servo driver). The communication is in a differential transmission format that complies with RS-485 electrical standard. The encoder will carry out specific operation based on the command request made by the Master. Acknowledgment of the command request is necessary before the encoder executes the requested operation, i.e. by checking the Start bit, information data field and Stop bit. Upon failing this checking, the command request will not be acknowledged and executed.

Figure 1 General transmission frames format on half duplex line

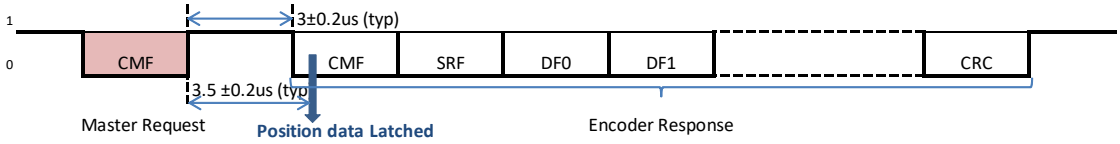


- **Start of transmission frames set:** The encoder will acknowledge as a valid Command Frame (CMF) upon detecting
  - the first logic of Low state “0” on the transmission line after idling state, and
  - the following 3 bits conform to a valid command identifier, indicating the start of transmission frame set,

  else, it will continue to search for the next available logic of low state ”0”.
- **End of transmission frames set:** After the Command Frame is detected, if there is no Start Bit after the End Bit of the last frame read, and no subsequent frame is detected, end of transmission frame set is concluded.
- **Idle state:** Idle state means a space between each transmission frames set and subsequent transmission frames. At idling state, logic of output in transmission line are kept to high state “1”.

Encoder Data Read Out Frame Sets Format and Timing

Figure 2 Encoder Data Read out frames set



Upon the Master issuing a CMF request, after 3.0 µs (typical), the encoder shall respond with Encoder Data Frames set with the following contents:

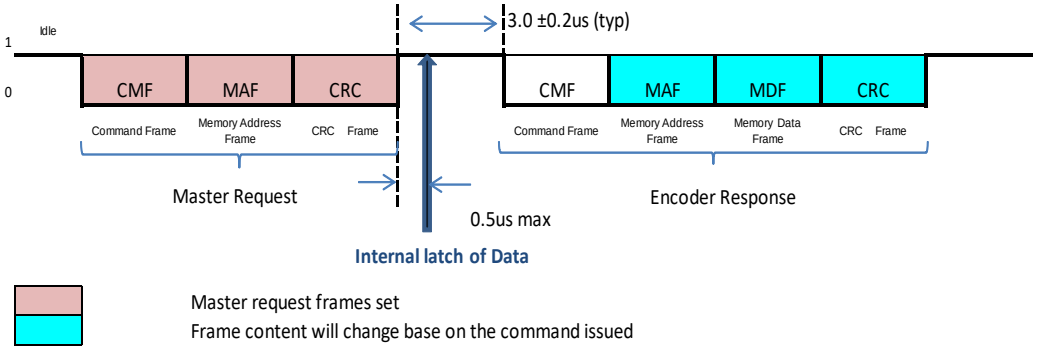
- CMF: corresponds to the Command Frame issued by the Master
- SRF: Status Response Frame
- DF^0~DF^7: Encoder Data Frames
- CRC: Cyclic Redundancy Check (CRC) frame

Encoder position calculation will be completed 3.5µs (typical) after the end bit of Master request CMF frame.

The encoder responded data frames set format are dependent on the requested operation by the Master, refer to Table 4.

EEPROM Data Read Out Frames Set Format and Timing

Figure 3 EEPROM Data Read out frames set

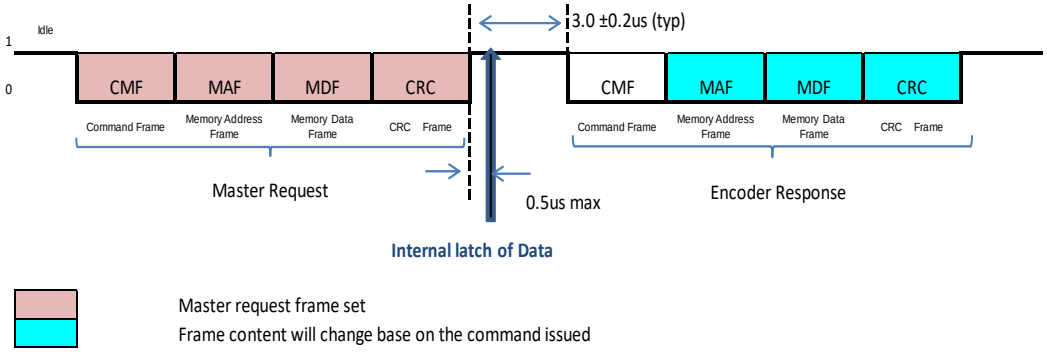


Content of transmission frames:-

- CMF: Command Frame (Same for both Master Command and Encoder Response)
- MAF: Memory Address Frame indicates the EEPROM memory location to Read.
- CRC: Cyclic Redundancy Check (CRC) checking
- MDF: Memory Data Frame contains the data read from EEPROM.

EEPROM Data Write Frames Set Format and Timing

Figure 4 EEPROM Data write frames set



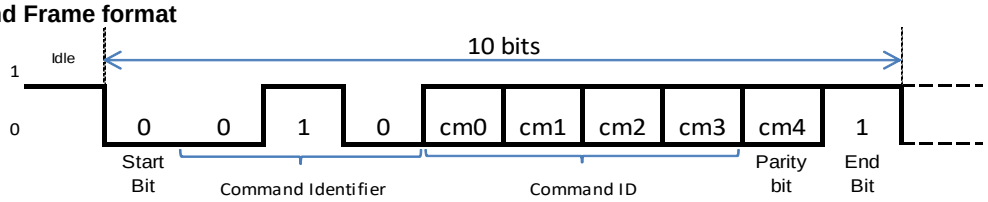
Content of transmission frames:-

- CMF: Command Frame (Same for both Master Command and Encoder Response)
- MAF: Memory Address Frame indicates the EEPROM memory location to write.
- MDF: Memory Data Frame contains the data to write to EEPROM.
- CRC: CRC checking.

Details Description of Data Frames

Command Frame (CMF)

Figure 5 Command Frame format



Content of CMF frame:-

- Start Bit: Indicating the start of Frame, always “0”
- Command Identifier: Indicate a valid command frame has been issued, defined as “010”.
- Command ID: Combination of bits defining command instructions, refer to Table 3 and Table 4
- Parity Bit: Parity check bit for Command ID, refer to Table 3.
- End Bit: Indicating end of Frame, always “1”

Command ID and Encoder Operation Definition

Table 3 Definition of Encoder Operation Command Codes and Parity bit

Encoder Operation	Command ID	Command ID Bits				Parity
		cm0	cm1	cm2	cm3	cm4
Encoder Information Read Out	0	0	0	0	0	0
	1	1	0	0	0	1
	2	0	1	0	0	1
	3	1	1	0	0	0
EEPROM Write	6	0	1	1	0	0
EEPROM Read	D	1	0	1	1	1
Clear All Errors	7	1	1	1	0	1
Single-Turn Counter Reset	8	0	0	0	1	1
Multi-Turn Counter Reset & Clear All Errors	C	0	0	1	1	0

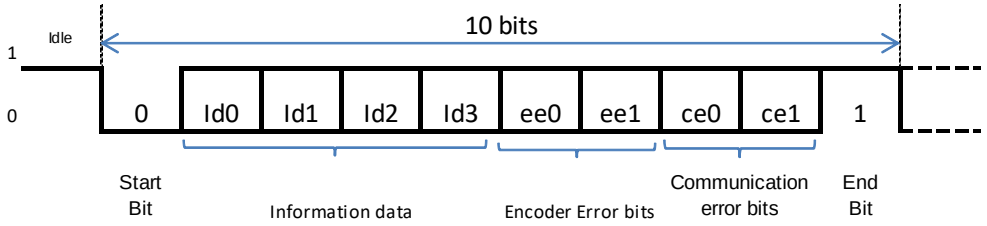
Description of Encoder Operation

Table 4 Description of encoder operation

Operation	Command ID	Description of Operation
Encoder Information Read Out	0, 1, 2, 3	Transmit Command ID code (Table 3) according to the List of Data Field (Table 4) to Encoder.
Single-Turn Counter Reset	8	Transmit request minimum 10 times consecutively at an interval of 40µs or more to the Encoder, where the motor shaft is in a stationary condition. Note).
		Single turn Zero position can be reset to any desired position.
		Upon successful completion of Zero Reset, the Zero position will be retained regardless of the presence of Vcc or battery backup supply.
Multi-Turn Counter Reset & All Error Clear	C	Transmit request minimum 10 times consecutively at an interval of 40µs or more to the Encoder, where the motor shaft is in a stationary condition. Note).
		Only Multi-turn counter will be reset (Single turn counter is not reset).
		All latched errors as described in Table 7 are reset at the same time.
Clear All Error	7	Transmit request minimum 10 times consecutively at interval of 40µs or more to the Encoder, where the motor shaft is in a stationary condition. Note).
		All latched errors as described in Table 7 are reset at the same time.
EEPROM Read	D	8 bits of data to be read from designated EEPROM address of User accessible memory area. Refer to Appendix A for recommended EERPOM read out process flow.
EEPROM Write	6	8 bits of data to be written into designated EEPROM address of User accessible area. Refer to Appendix B for recommended EERPOM writing process flow and Data content confirmation.

Status Response Frame (SRF)

Figure 6 SRF frame format



Content of SRF frame:-

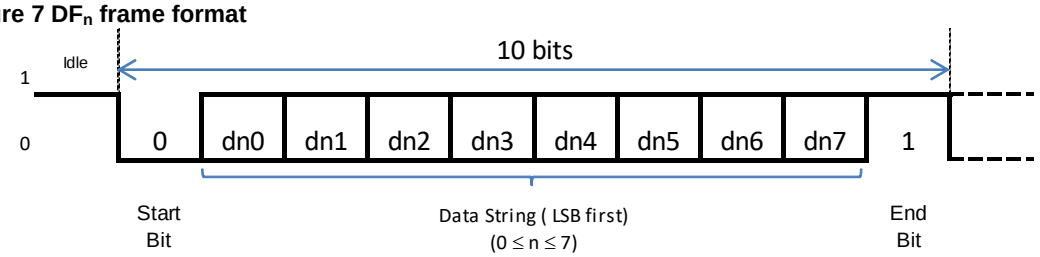
- Start Bit: Indicating the start of Frame, always “0”
- Information Data: Defined as “0000”
- Encoder Error Bits: Return with state “1” if encoder error is detected, referring to Table 5
- Communication Error Bits: Return with state “1” if communication error detected, referring to Table 5.
- End bit: Indicating the end of Frame, always “1”

Table 5 Encoder Error and Communication Error Descriptions

Logic When Error Detected	Error Flag	Error Description
Encoder Error Bits "1"	ee0	Encoder ST Counting Error
	ee1	Multi-turn Count Error OR Battery Supply Error OR Battery Supply Alarm detected
Communication Error Bits "1"	ce0	Parity Error detected in Master Request Frames set
	ce1	End Bit Error detected in Master Request Frames set.

Encoder Data Frame (DF_n)

Figure 7 DF_n frame format



Content of DF_n frame:-

- Start Bit: Indicating the start of Frame, always “0”
- dn^0~dn^7: 8 bits data set with LSB first in sequence.
- End Bit: Indicating end of Frame, always “1”

Description of Data Frames with Respective Command ID

Table 6 Data frames content with respective command ID

Command ID	DF0	DF1	DF2	DF3	DF4	DF5	DF6	DF7
0	STC0	STC1	STC2					
1	MTC0	MTC1	MTC2					
2	ENID							
3	STC0	STC1	STC2	ENID	MTC0	MTC1	MTC2	ERRF
7	STC0	STC1	STC2					
8	STC0	STC1	STC2					
C	STC0	STC1	STC2					

STCn: Single Turn counts, LSB of the Single Turn counts is located in STC0 and MSB of the counts data is located in STC2. Combining STC0~STC2 will provide a total to 24 bits of Single Turn data.
For Single Turn 23 bits encoder option, the MSB of STC2 is fixed to “0”, hence giving a total of 23 bits Single Turn data.
For Single Turn 17 bits encoder option, the higher 7 bits of STC2 is fixed to “0”, hence giving a total of 17 bits Single Turn data.

MTCn : Multi Turn counts, LSB of the multi-turn counts is located in MTC0 and MSB of the counts data is located in MTC2. Combining MTC0~MTC2 will provide a total to 24 bits of multi-turn data. For 16 bits multi-turn counting, MTC2 are fixed to “00”, hence giving a total of 16 bits multi-turn data.

ENID : Encoder Single Turn bits identification
For Single Turn 23 bits encoder option, ENID is fixed as “17h”
For Single Turn 17 bits encoder option, ENID is fixed as “11h”
ERRF : Encoder Error Flags. Refer to Table 7.

Table 7 Error flag bits definition

Bit Value	ERRF Bit							
	DF7-0	DF7-1	DF7-2	DF7-3	DF7-4	DF7-5	DF7-6	DF7-7
0	No Error	Not in use	No Error	No Error	Not in use	No Error	No Error	No Error
1	Over Speed Error (OSPE)	Not in use	Single-turn Counting Error (STCE)	Multi turn Counter Overflow (MTCO)	Not in use	Multi-turn Counting Error (MTCE)	Battery Supply Error (BSE)	Battery Supply Alarm (BSA)

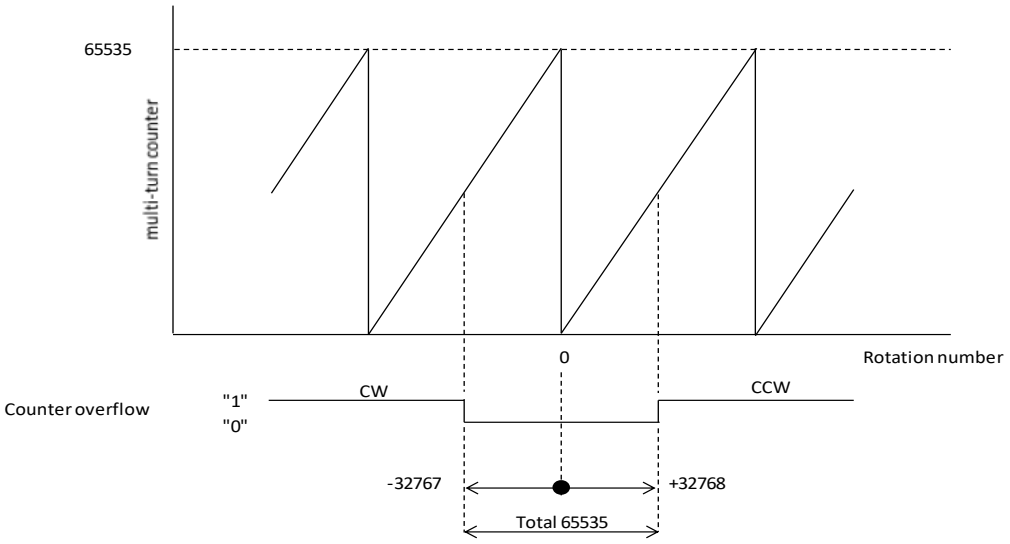
Table 8 Encoder alarms description

Error Flags	Detection Mode	Description	Reset Method
Over Speed Error	Battery mode	To detect over speed and wrong multi-turn counting during Battery mode. The error flag is latched and will be transmitted once encoder enter normal mode. 1: Shaft rotation speed > 6000 rpm and wrong multi-turn count detected 0: Condition 1) Shaft rotation speed < 6000 rpm or, Condition 2) Shaft rotation speed > 6000 rpm but no wrong multi-turn count detected. This error flag are Not defined if speed > 14000 rpm.	Perform all error clear
Single-turn Counting Error	Normal mode	To check integrity of single-turn position data calculation. 1: Error detected in single-turn position counting. 0: No Error detected.	Cycle power encoder
Counter Overflow Error	Battery mode	To indicate multi-turn counter overflow condition. (Refer to Figure 13). The error flag is latched and will be transmitted out once encoder entering normal mode. 1: Multi turn counter overflowed. 0: Multi turn counter Not overflowed.	Perform MT counter reset and all error clear
Multi-turn Counting Error	Normal mode	To check integrity of multi turn position data counting. The error flag is latched. 1: Error detected in multi turn position counting 0: No Error detected	Perform MT counter reset and all error clear
Battery Supply Error	Battery mode	To check backup battery supply low voltage condition. The error flag is latched and will be transmitted out once encoder entering normal mode. 1: Battery voltage is lower than 2.9 ±0.25V 0: Battery voltage is higher than 2.9 ±0.25V	Perform all error clear
Battery Supply Alarm	Normal mode	To check backup battery supply low voltage condition. The error flag will be automatically cleared once the battery voltage return to normal value. 1: Battery voltage is lower than 3.1 ±0.1V 0: battery voltage is higher than 3.1 ±0.1V	Error flag automatically clear once battery voltage return to normal

LED Error	Normal mode	To indicate if LED current is out of operating range. 1: LED out of operating range. 0: LED within operating range.	Cycle power encoder
Lissajous Error	Normal mode	To check integrity of ADC Sin and Cos signals by means of Lissajous specifications. 1: Lissajous out of specification. 0: Lissajous within specification.	Cycle power encoder

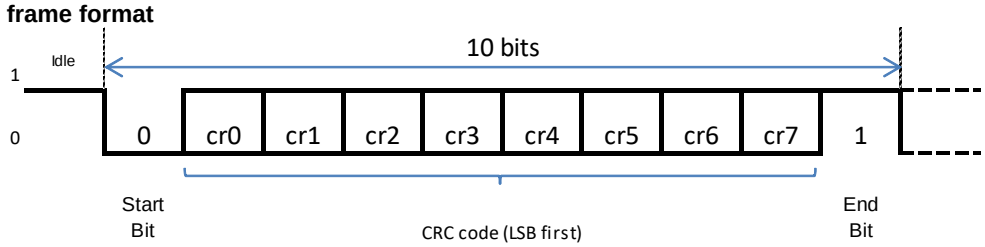
Multi-turn Counter Overflow Flag Explanation

Figure 8 Relation between multi-turn counting and over flow flag



Cyclic Redundancy Check Frame (CRC)

Figure 9 CRC frame format



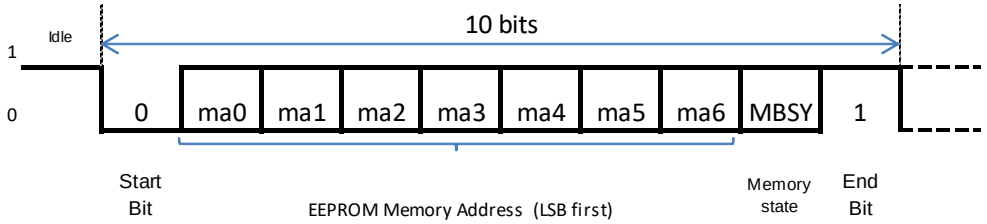
Content of CRC frame:-

- Start Bit: Indicating the start of frame, always “0”
- cr^{0}~^{cr7}: 8 bits of CRC data set with LSB first in the sequence.
- End Bit: Indicating the end of frame, always “1”

NOTE The CRC code is generated per the equation of $G(X) = X^{8} + 1$ (X = cr0 ~cr7)

Memory Address Frame (MAF)

Figure 10 MAF frame format

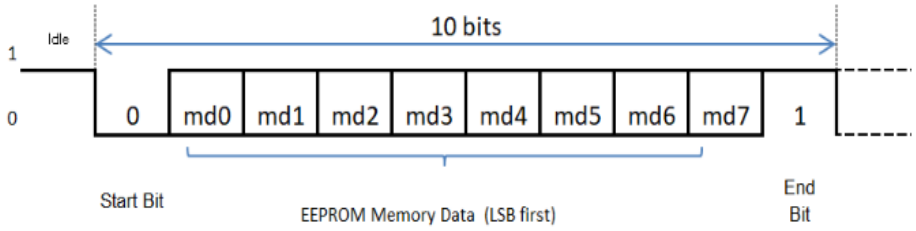


Content of MAF frame:-

- Start Bit: Indicating the start of frame, always “0”
- ma^0~ma^6: 7 bits Memory Address data set with LSB first in the sequence.
- MBSY: Memory Access busy status Flag, refer to Table 9.
- End Bit: Indicating the end of frame, always “1”

Memory Data Frame (MDF)

Figure 11 MDF frame format



Content of MDF frame:-

- Start Bit : Indicating the start of frame, always “0”
- md^0~md^7: 8 bits EEPROM Memory data set with LSB first in the sequence.
- End Bit: Indicating the end of frame, always “1”

Table 9 MBSY status definition

EEPROM Access Operation	Master Command	Encoder Response			Remarks
	MBUSY Value in MAF	MBUSY Value in MAF	Content of MAF	Content of MDF	
EEPROM Read	0	0	EEPROM Address to read	Correct Data read from EEPROM	EEPROM read completed
		1	EEPROM Address to read	"00"	EEPROM busy, accessing in progress, subsequent request will not be accepted
EEPROM Write	0	0	EEPROM Address to write	Data to write in to EEPROM	EEPROM not busy, Write request accepted.
		1	EEPROM Address to write	"00"	EEPROM is busy, accessing in progress, subsequent request will not be accepted

EEPROM User Accessible Memory Area

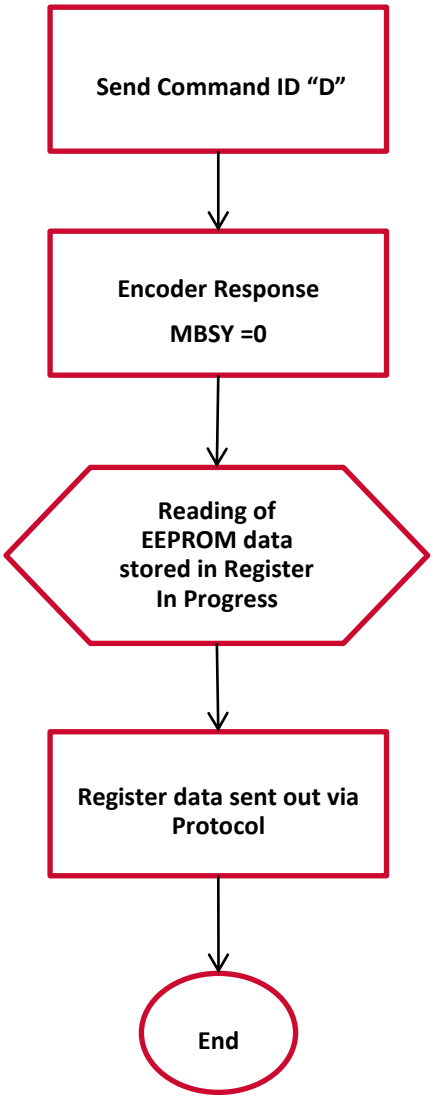
Table 10 User Accessible Memory Area

EEPROM Address	EEPROM Bank				
	0	1	2	3	4
00h					
01h					
02h					
03h					
7Dh					
7Eh					
7Fh					

NOTE

1. Total 5 banks, with 127 addresses each, are allocated for User access, as highlighted in green.
2. All User accessible addresses are pre-programed to “00” prior to shipment.
3. The active bank numbers are specified in address 7Fh, bank change is done by writing to address 7Fh.
4. Once the bank value is changed, allow an 18ms delay.
5. Typical EEPROM Read time is 200µs minimum.
6. Typical EEPROM Write time is 6ms minimum.
7. Permissible EEPROM writing cycle is 1,000,000 times.
8. Please refer to Appendix A & B for further details on EEPROM Read/Write procedures.

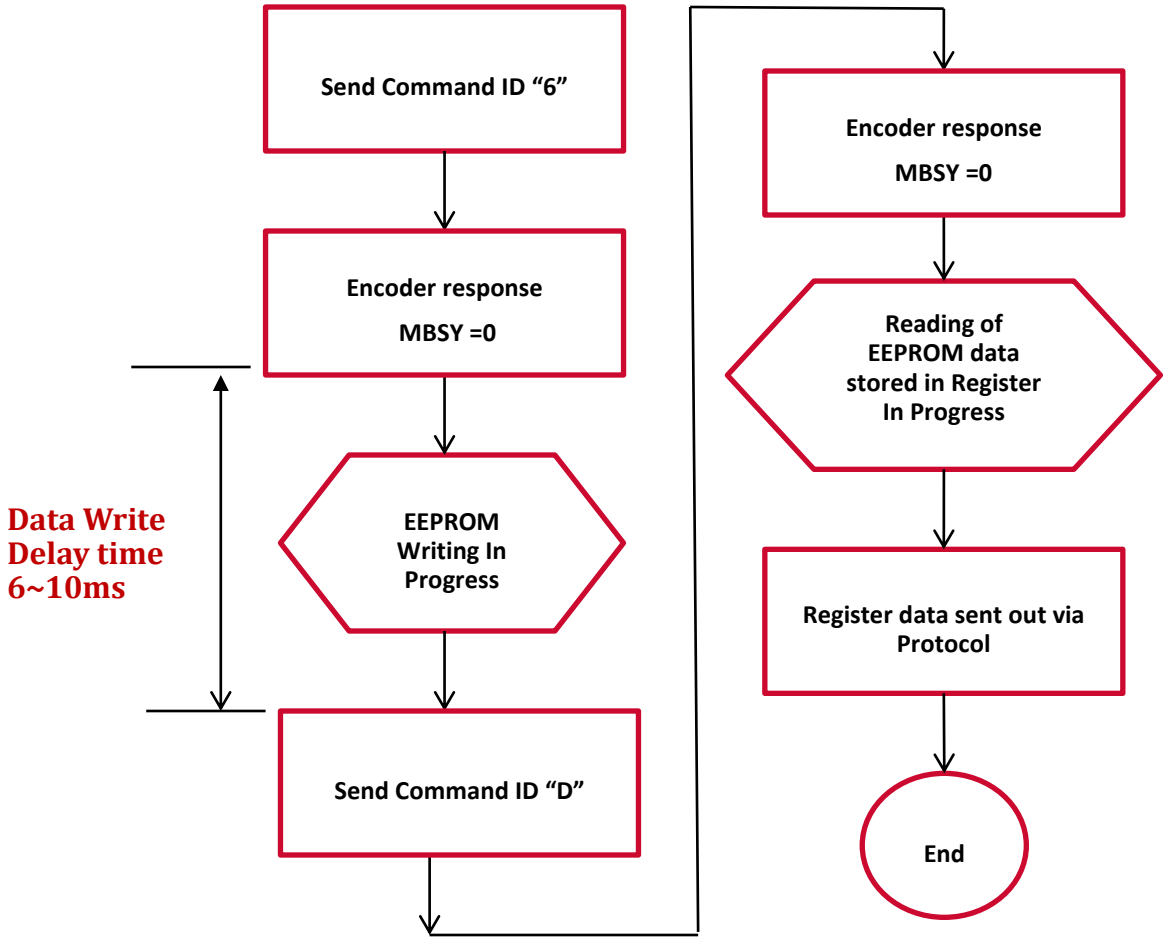
Appendix A



NOTE

1. Each EEPROM reading requires sending a Command ID "D" from the Master.
2. A Command ID "D" from master will initiate reading Data from Register, MBSY flag will return value "0".

Appendix B



NOTE

1. Every time when issuing of Command ID 6 request, the MDF content writing may not be confirmed even though the MBSY flag returns a value of "0".
2. It is recommended to issue a Command ID "D" request , 6~10ms after the issuance of EEPROM write request to read the designate MDF data for confirmation if the correct data has been successfully written.