35AT-4B25 Series

25-Bit Single-Turn with Battery Backup Multi-Turn RS485 Absolute Encoder

Description and General Specification

This document provides an explanation of the RS485 software specification for the 25-bit 35AT-4B25 series encoders.

Table 1 General Specification of the RS485 Serial Communication

| Item	Specification	Note
Transmission Type	Differential Transceiver	
Communication Type	Half duplex	Recommended Transceiver: ISL8485E or equivalent
Transmission Code Type	Binary, Non Return Zero (NRZ) code	
Synchronization Type	Asynchronous	
Communication Baud Rate	2.5/5.0/10Mbps	Default 2.5Mbps
Frame Length	10 bits/Frame	
Transmission Error Checking	8 bits CRC	CRC equation $G(X) = X^8 + 1$ $X = cr0 \sim cr7$

Definition of Encoder Operating Mode

Mode	Definition	VCC (Typical)	BATPWR (Typical)	Remarks
Power off mode	This is non-operation state of the encoder, where the main power supply, Vcc line and battery backup supply are not connected.	0V	0V	Before installation
Normal mode	This is normal operation state of the encoder, when main power supply Vcc is available. At this state, counting of single turn position, counting of multi-turn position and data transmission between encoder and Host are possible.	5V	3.6V	
Battery mode	This is battery backup operation stage, where the encoder is powered up by the backup battery connected to BATPWR input. At this state, only multi-turn counting is available.	0V	3.6V	

Table 2 Definition of Encoder Operating Mode

Transmission Frames between Host and Encoder

Overview of Communications

A one-to-one half-duplex serial communication is established between the encoder and the Host (e.g. servo driver). The communication is in a differential transmission format. The encoder will carry out specific operation based on the command request made by the Host. Acknowledgment of the command request is necessary before the Client Encoder executes the requested operation, i.e. by checking the Start bit, information data field and Stop bit. Upon failing this checking, the command request will not be acknowledged and executed.
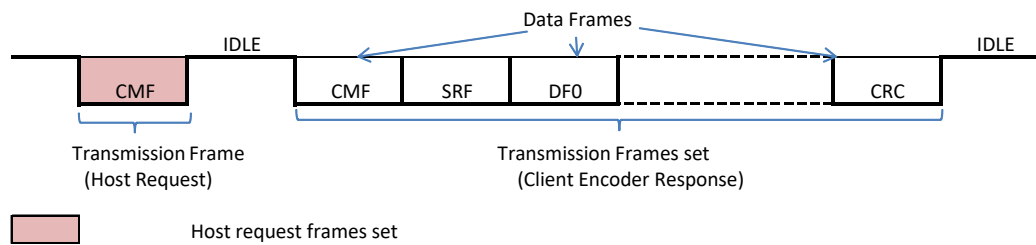
Figure 1 General transmission frames format on half duplex line

- **Start of transmission frames set:** The encoder will acknowledge as a valid Command Frame (CMF) upon detecting
  - the first logic of Low state "0" on the transmission line after idling state, and
  - the following 3 bits conform to a valid command identifier, indicating the start of transmission frame set,

  else, it will continue to search for the next available logic of low state "0".

- **End of transmission frames set:** After the Command Frame is detected, if there is no Start Bit after the End Bit of the last frame read, and no subsequent frame is detected, end of transmission frame set is concluded.

- **Idle state:** Idle state means a space between each transmission frames set and subsequent transmission frames. At idling state, logic of output in transmission line are kept to high state "1".

Encoder Data Read Out Frame Sets Format and Timing
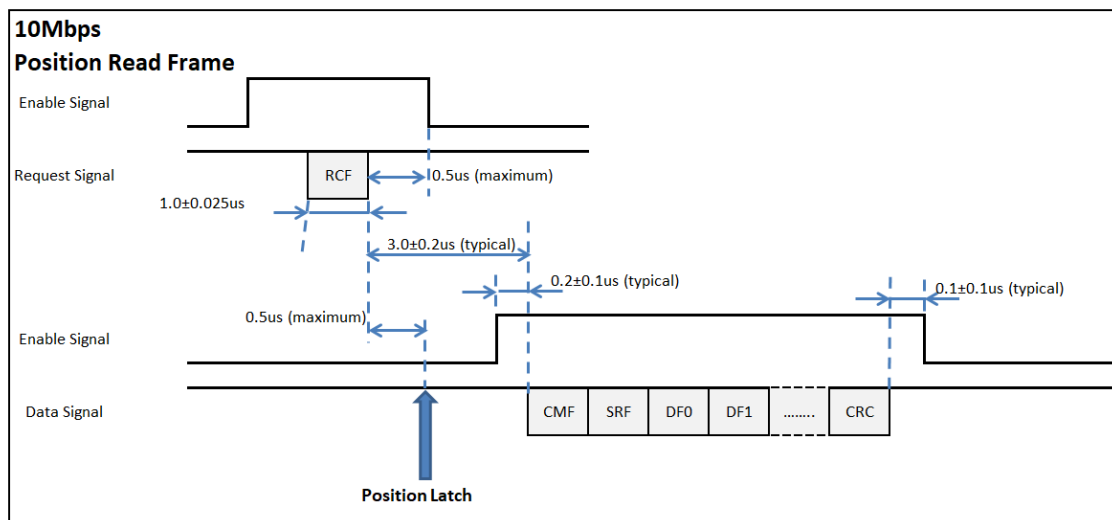
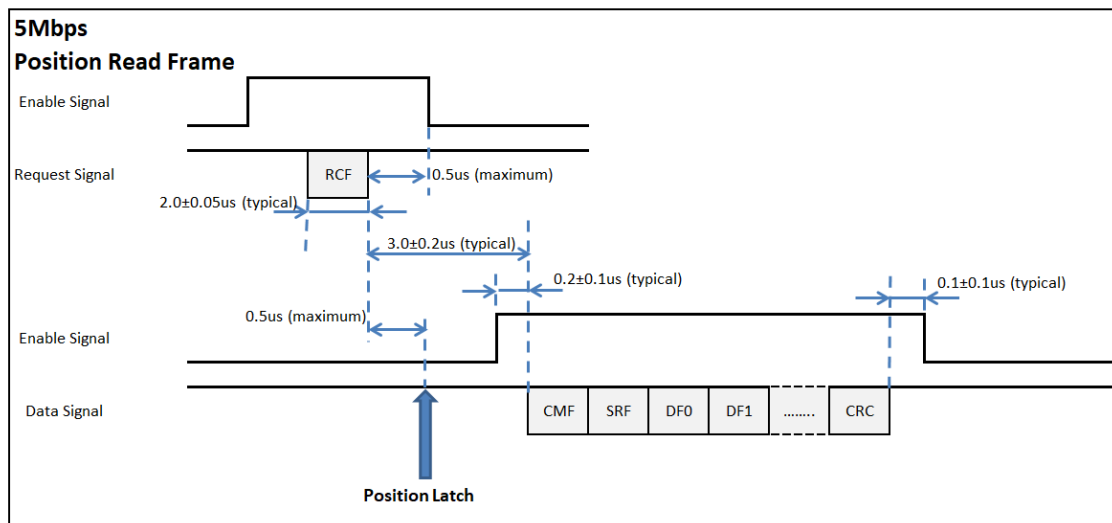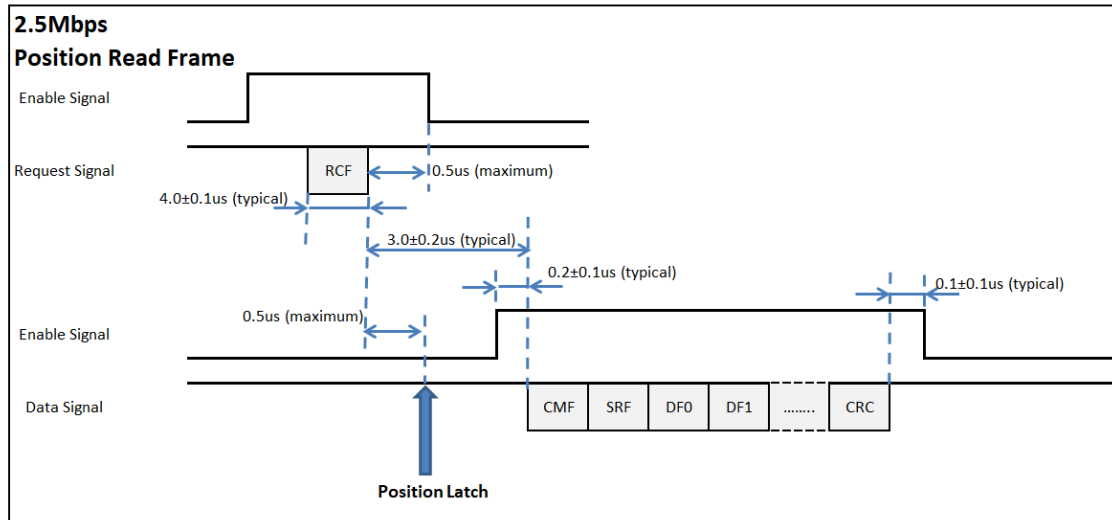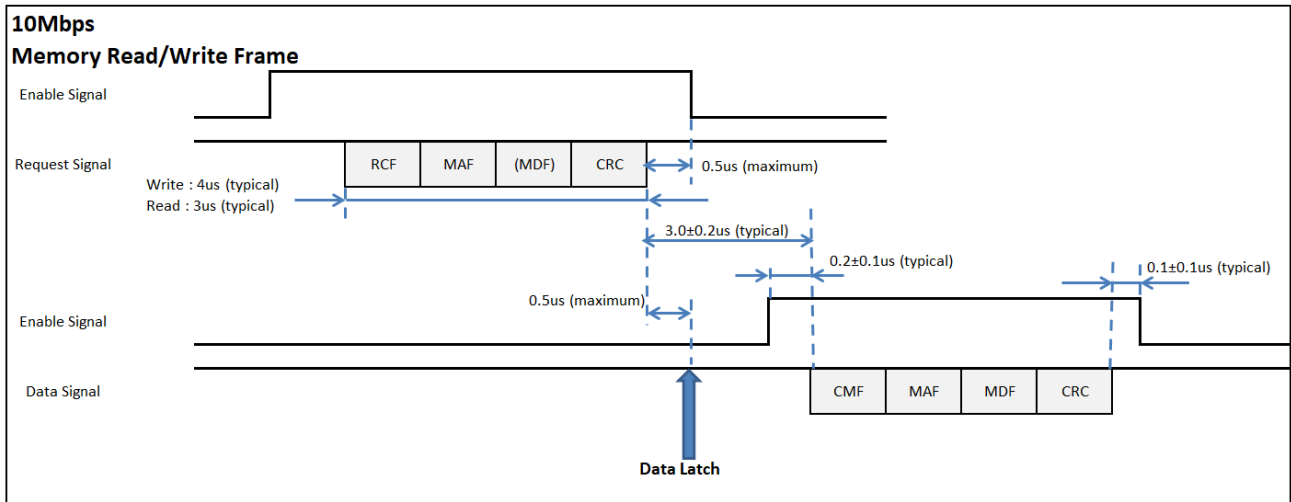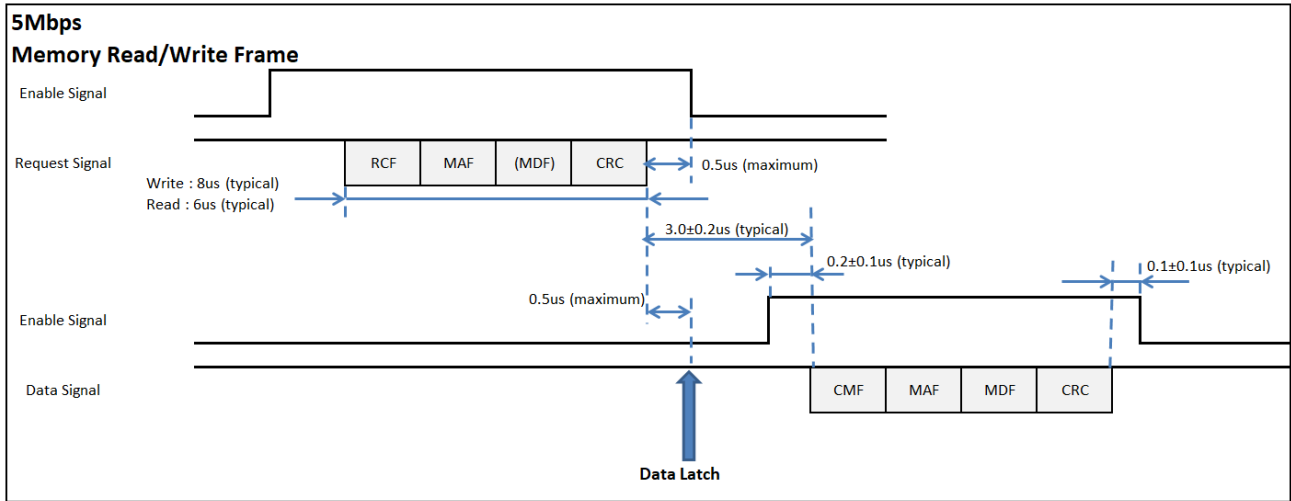**Figure 1 Encoder position data read out frames set**

Figure 2 Encoder memory data Read & Write frames set
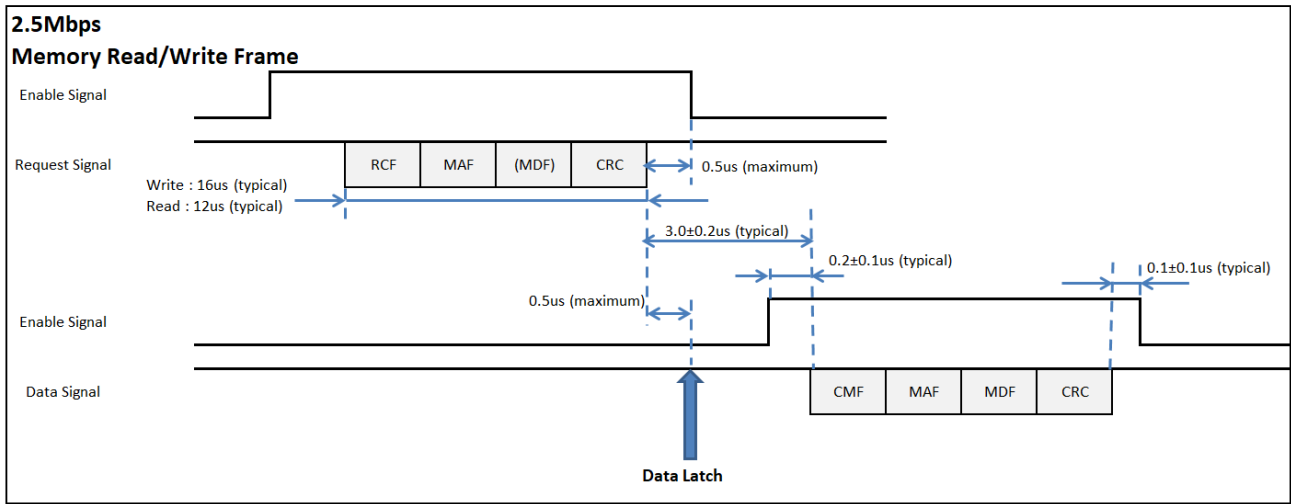
Upon the Host issuing a CMF request, after 3.0 µs (typical), the Client Encoder shall respond with Encoder Data Frames set with the following contents:

- CMF: corresponds to the Command Frame issued by the Host
- SRF: Status Response Frame
- $DF^0 \sim DF^7$: Encoder Data Frames
- CRC: Cyclic Redundancy Check (CRC) frame

Encoder position calculation will be latched within 0.5µs (typical) after the end bit of Host request CMF frame.

The Client Encoder responded data frames set format are dependent on the requested operation by the Host, refer to Table 4.

EEPROM Data Read Out Frames Set Format and Timing

Figure 3 EEPROM data read out frames set

Content of transmission frames:-

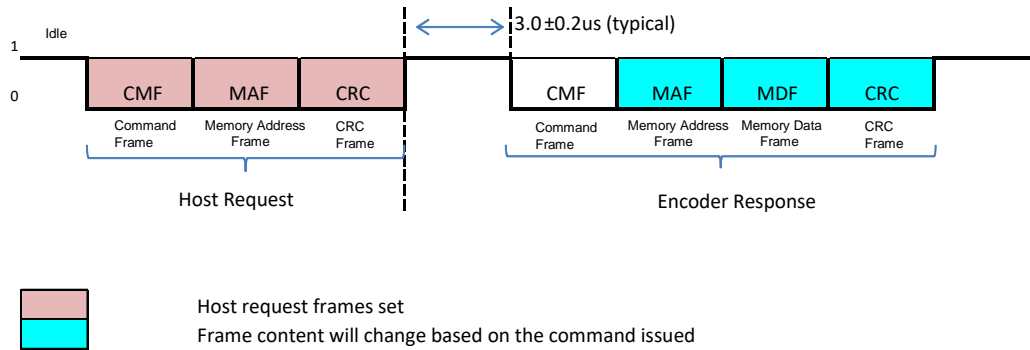- CMF: Command Frame (Same for both Host Command and Encoder Response)
- MAF: Memory Address Frame indicates the EEPROM memory location to Read.
- CRC: Cyclic Redundancy Check (CRC) checking
- MDF: Memory Data Frame contains the data read from EEPROM.

EEPROM Data Write Frames Set Format and Timing

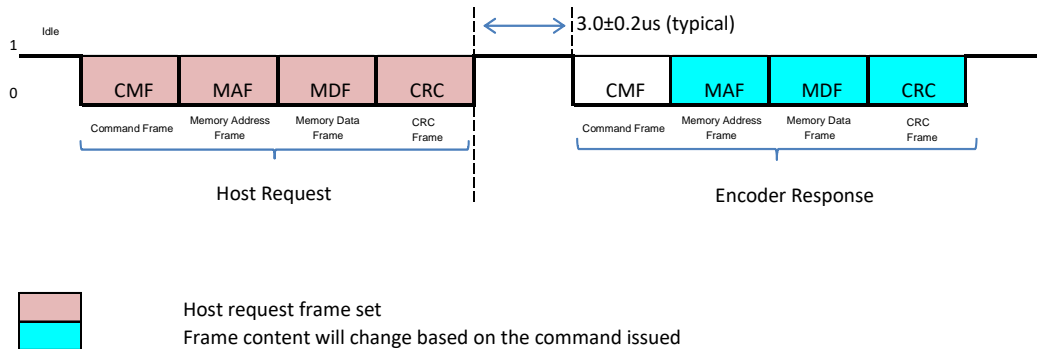**Figure 4 EEPROM data write frames set**

Content of transmission frames:-

- CMF: Command Frame (Same for both Host Command and Encoder Response)
- MAF: Memory Address Frame indicates the EEPROM memory location to write.
- MDF: Memory Data Frame contains the data to write to EEPROM.
- CRC: CRC checking.

Details Description of Data Frames

Command Frame (CMF)

Figure 5 Command Frame format
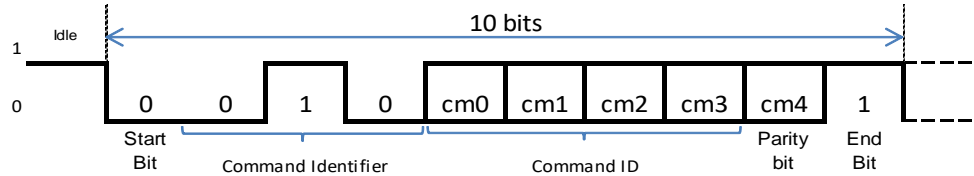
Content of CMF frame:-

- Start Bit: Indicating the start of Frame, always "0"
- Command Identifier: Indicate a valid command frame has been issued, defined as "010".
- Command ID: Combination of bits defining command instructions, refer to Table 3 and Table 4
- Parity Bit: Parity check bit for Command ID, refer to Table 3.
- End Bit: Indicating end of Frame, always "1"

Command ID and Encoder Operation Definition

Table 3 Definition of encoder operation command codes and parity bit

| Encoder Operation	Command ID	Encoder Sync Code			Data ID Bits				Parity	HEX
		BIT 0	BIT 0	BIT 0	CM0	CM1	CM2	CM3	CM4	
Position Information	2	0	1	0	0	1	0	0	1	92
	3	0	1	0	1	1	0	0	0	1A
	4	0	1	0	0	0	1	0	1	A2
	5	0	1	0	1	0	1	0	0	2A
Memory Write	6	0	1	0	0	1	1	0	0	32
Memory Read	D	0	1	0	1	0	1	1	1	EA
Alarm Clear	7	0	1	0	1	1	1	0	1	BA
Single-Turn Position Zero Reset	8	0	1	0	0	0	0	1	1	C2
Multi-turn Counter Reset & Alarm Clear	C	0	1	0	0	0	1	1	0	62

Description of Encoder Operation

Table 4 Description of encoder operation

Operation	Command ID	Description of Operation
Encoder Information Read Out	2, 3, 4, 5	Transmit Command ID code (Table 3) according to the List of Data Field (Table 4) to Encoder.
Single-Turn Counter Reset	8	Transmit request minimum 10 times consecutively at an interval of 40µs or more to the Encoder, where the motor shaft is in a stationary condition.
		Single turn Zero position can be reset to any desired position.
		Upon successful completion of Zero Reset, the Zero position will be retained regardless of the presence of Vcc or battery backup supply.
Multi-Turn Counter Reset & All Error Clear	C	Transmit request minimum 10 times consecutively at an interval of 40µs or more to the Encoder, where the motor shaft is in a stationary condition. Note).
		Only Multi-turn counter will be reset (Single turn counter is not reset).
		All latched errors as described in Table 7 are reset at the same time.
Clear All Error	7	Transmit request minimum 10 times consecutively at interval of 40µs or more to the Encoder, where the motor shaft is in a stationary condition.
		All latched errors as described in Table 7 are reset at the same time.
EEPROM Read	D	8 bits of data to be read from designated EEPROM address of User accessible memory area. Refer to Appendix A for recommended EERPOM read out process flow.
EEPROM Write	6	8 bits of data to be written into designated EEPROM address of User accessible area. Refer to Appendix B for recommended EERPOM writing process flow and Data content confirmation.

Status Response Frame (SRF)

Figure 6 SRF frame format
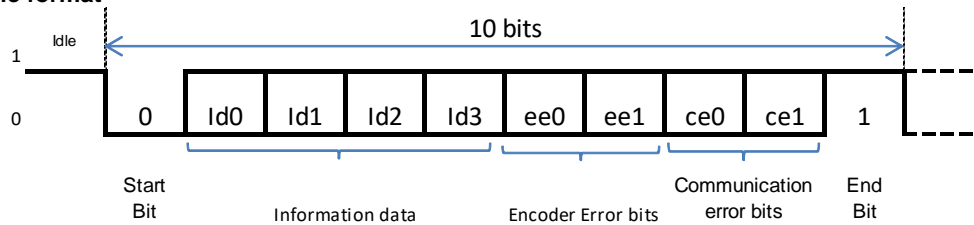
Content of SRF frame:-

- Start Bit: Indicating the start of Frame, always "0"
- Information Data: Defined as "0000"
- Encoder Error Bits: Return with state "1" if encoder error is detected, referring to Table 5
- Communication Error Bits: Return with state "1" if communication error detected, referring to Table 5.
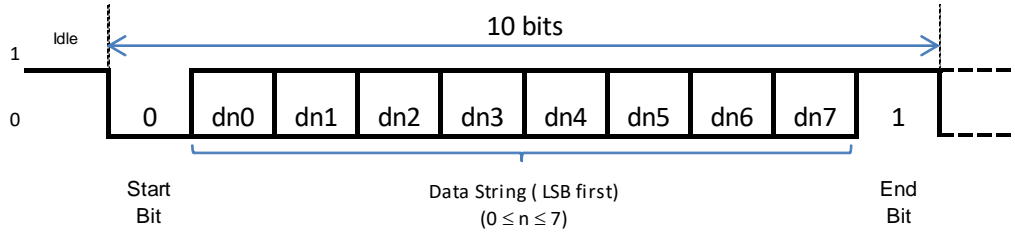- End bit: Indicating the end of Frame, always "1"

Table 5 Encoder error and communication error descriptions

Logic When Error Detected	Error Flag	Error Description
Encoder Error Bits "1"	ee0	Encoder ST Counting Error
	ee1	Multi-turn Count Error OR Battery Supply Error OR Battery Supply Alarm detected OR Temperature Alarm
Communication Error Bits "1"	ce0	Parity Error detected in Host Request Frames set
	ce1	End Bit Error detected in Host Request Frames set.

Encoder Data Frame (DF$_n$)

Figure 7 DF$_n$ frame format

Content of DF$_n$ frame:-

- Start Bit: Indicating the start of Frame, always "0"
- dn^0~dn^7: 8 bits data set with LSB first in sequence.
- End Bit: Indicating end of Frame, always "1"

Description of Data Frames with Respective Command ID

Table 6 Client responded data frames content with respective command ID

ID	CF	SF/ ADF	DF0/ EDF	DF1	DF2	DF3	DF4	DF5	DF6	DF7	CRC	Frame Size
2	CF	SF	ENID								Include CRC	4
3	CF	SF	STC0	STC1	STC2	ENID	STC3	MTC0	MTC1	ERRF		11
4	CF	SF	STC0	STC1	STC2	STC3						7
5	CF	SF	STC0	STC1	STC2	STC3	MTC0	MTC1				9
6	CF	MAF	MDF									4
7	CF	SF	STC0	STC1	STC2							6
8	CF	SF	STC0	STC1	STC2							6
C	CF	SF	STC0	STC1	STC2							6
D	CF	MAF	MDF									4

NOTE   **STCn** : Single-turn counts, LSB of the single-turn counts is located in STC0 and MSB of the counts data is located in STC3. 7 bits LSB of STC0 are fixed to "0". Combining STC0~STC3 will provide a maximum total of 25 bits single-turn data.

                 MTCn : Multi-turn counts, LSB of the multi-turn counts is located in MTC0 and MSB of the counts data is located in MTC1. Combining MTC0~MTC1 will provide a maximum total of 16 bits multi-turn data.

ENID : Encoder Single-turn bits identification in 8-bit format. For Single-turn 25-bit output is set to "19h".

ERRF : Encoder Error Flags in 8-bit format. Refer to Table 7.

Table 7 Error flag bits definition

| Bit Value	ERRF Bit							
	DF7-0	**DF7-1**	**DF7-2**	**DF7-3**	**DF7-4**	**DF7-5**	**DF7-6**	**DF7-7**
0	No Error	Not in use	No Error	No Error	No Error	No Error	No Error	No Error
1	Over Speed Error (OSPE)	Not in use	Single-turn Counting Error (STCE)	Multi turn Counter Overflow (MTCO)	Temp Error (TE)	Multi-turn Counting Error (MTCE)	Battery Supply Error (BSE)	Battery Supply Alarm (BSA)

Table 8 Encoder alarms description

Error Flags	Detection Mode	Description	Reset Method
Over Speed Error	Battery mode	To detect over speed and wrong multi-turn counting during Battery mode. The error flag is latched and will be transmitted once encoder enter normal mode. 1: Shaft rotation speed > 6000 rpm and wrong multi-turn count detected 0: Condition 1) Shaft rotation speed < 6000 rpm or, Condition 2) Shaft rotation speed > 6000 rpm but no wrong multi-turn count detected. This error flag are Not defined if speed > 14000 rpm.	Perform all error clear
Single-turn Counting Error	Normal mode	To check integrity of single-turn position data calculation. 1: Error detected in single-turn position counting. 0: No Error detected.	Cycle power encoder
Counter Overflow Error	Battery mode	To indicate multi-turn counter overflow condition. (Refer to Figure 13). The error flag is latched and will be transmitted out once encoder entering normal mode. 1: Multi turn counter overflowed. 0: Multi turn counter Not overflowed.	Perform MT counter reset and all error clear
Multi-turn Counting Error	Normal mode	To check integrity of multi turn position data counting. The error flag is latched. 1: Error detected in multi turn position counting 0: No Error detected	Perform MT counter reset and all error clear
Battery Supply Error	Battery mode	To check backup battery supply low voltage condition. The error flag is latched and will be transmitted out once encoder entering normal mode. 1: Battery voltage is lower than 2.9 ±0.25V 0: Battery voltage is higher than 2.9 ±0.25V	Perform all error clear
Battery Supply Alarm	Normal mode	To check backup battery supply low voltage condition. The error flag will be automatically cleared once the battery voltage return to normal value. 1: Battery voltage is lower than 3.1 ±0.1V 0: battery voltage is higher than 3.1 ±0.1V	Error flag automatically clear once battery voltage return to normal

Error Flags	Detection Mode	Description	Reset Method
Temp Error	Normal mode	To indicate the detected ambient temperature exceeds the maximum preset limit (default: 110 degrees C). 1: temperature above preset limit. 0: temperature below preset limit.	Perform all error clear once temperature drops below the preset limit

Multi-turn Counter Overflow Flag Explanation

Figure 8 Relation between multi-turn counting and over flow flag
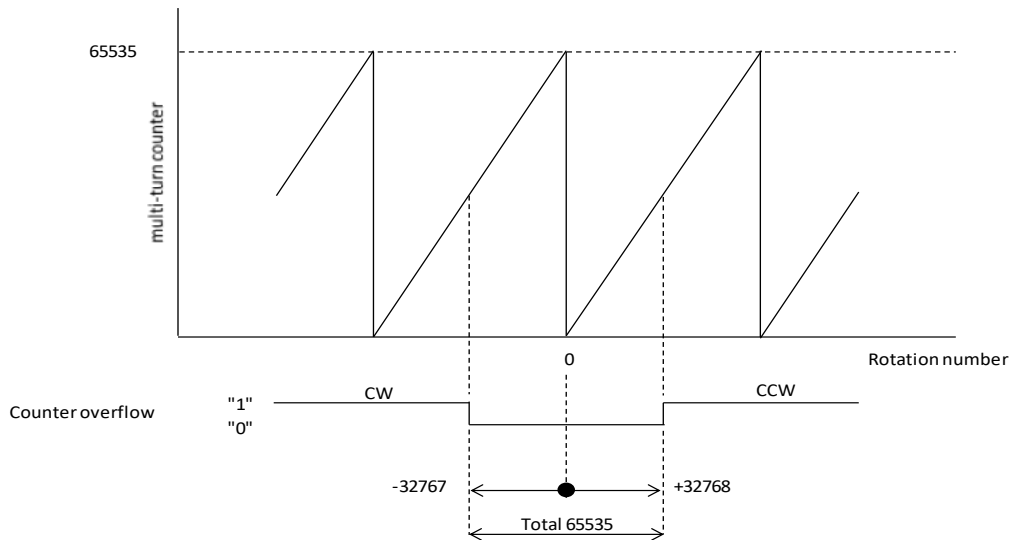
Cyclic Redundancy Check Frame (CRC)

Figure 9 CRC frame format
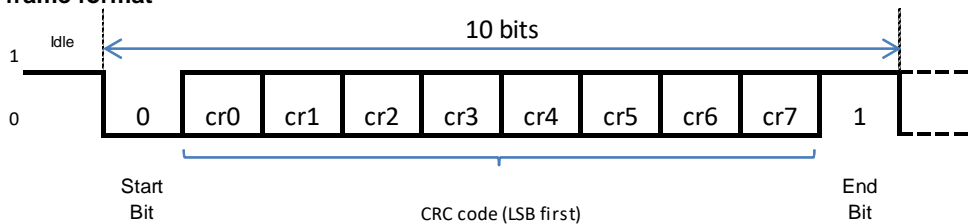
Content of CRC frame:-

- Start Bit: Indicating the start of frame, always "0"
- $cr_0 \sim cr_7$: 8 bits of CRC data set with LSB first in the sequence.
- End Bit: Indicating the end of frame, always "1"

NOTE   The CRC code is generated per the equation of $G(X) = X^8 + 1$ ($X = cr0 \sim cr7$)

Memory Address Frame (MAF)

Figure 10 MAF frame format

Content of MAF frame:-

- Start Bit: Indicating the start of frame, always "0"
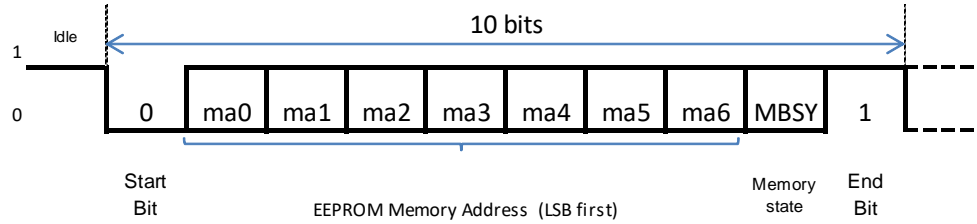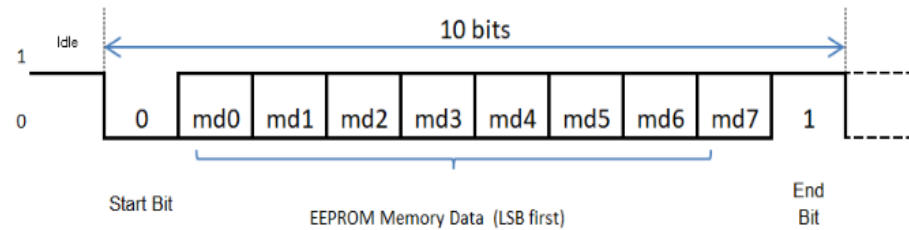- ma^0~ma^6: 7 bits Memory Address data set with LSB first in the sequence.
- MBSY: Memory Access busy status Flag, refer to Table 9.
- End Bit: Indicating the end of frame, always "1"

Memory Data Frame (MDF)

Figure 11 MDF frame format

Content of MDF frame:-

- Start Bit : Indicating the start of frame, always "0"
- md^0~md^7: 8 bits EEPROM Memory data set with LSB first in the sequence.
- End Bit: Indicating the end of frame, always "1"

Table 9 MBSY status definition

EEPROM Access Operation	Host Command	Encoder Response			Remarks
	MBUSY Value in MAF	MBUSY Value in MAF	Content of MAF	Content of MDF	
EEPROM Read	0	0	EEPROM Address to read	Correct Data read from EEPROM	EEPROM read completed
		1	EEPROM Address to read	"00"	EEPROM busy, accessing in progress, subsequent request will not be accepted
EEPROM Write	0	0	EEPROM Address to write	Data to write in to EEPROM	EEPROM not busy, Write request accepted.
		1	EEPROM Address to write	"00"	EEPROM is busy, accessing in progress, subsequent request will not be accepted

Temperature Sensor (Optional)

For the setting of temperature values and alarms, the configuration is as listed in Table 10 below. The temperature upper limit is defaulted to 0x6E, which is 110 °C, referenced to the ambient temperature as measured by the 35AT encoder ASIC.

Table 10 Temperature Sensor Setting

RS485			Temperature Sensor								Default [hex]
Page	Address		Bit								
[dec]	[dec]	[hex]	7	6	5	4	3	2	1	0	
7	2	0x02	Temperature Upper Limit Offset [7:0]								0x00
	3	0x03	Temperature Offset [7:0]								0x00
	4	0x04	Temperature Upper Limit [7:0]								0x6E
	5	0x05	Temperature Output Data (Read only register)								-

Encoder temperature readout bit, example of the data as 2's complement is listed as Table 1.

Table 1 Temperature Sensor Data

Temperature°C	TEMP[7:0]
-64	1100 0000
-50	1100 1110
-20	1110 1100
-1	1111 1111
0	0000 0000
1	0000 0001
10	0000 1010
25	0001 1001
50	0011 0010
85	0101 0101
127	0111 1111
159	1001 1111
191	1011 1111

NOTE

1. *Minimum support range for temperature output is -64°C.

2. Negative values are from -1°C to -64°C only.

3. The maximum positive value is 191°C.

4. Alternative temperature readout is by accessing memory register at Page 7 Address 0x05 (refer to Table 10).

Table 2 below is an example based on an initial Alarm (0x04) setting of 110 °C. The temperature offset can be a positive or negative value.

Table 2 Temperature sensor offset setting example

Case	Offset Value (Decimal)	Temperature Upper Limit Offset (hex) 0x02	Temperature Offset (hex) 0x03	Temperature Upper Limit (hex) 0x04	Temp Output Data (Dec) 0x05	Alarm Trigger
1	0	0	0	6E	109	N
					110	Y
					111	Y
2	10	0A	0A	6E	109	N
					110	Y
					111	Y
3	-1	0	FF	6E+01	109	N
					110	Y
					111	Y
4	-10	0	F6	6E+0A	109	N
					110	Y
					111	Y

NOTE

1. No offset scenario.
2. If the temperature offset (0x03) is positive value, then the Temp. Upper Limit Offset (0x02) is also set to the same value.
3. If the temperature offset (0x03) is negative value, then the absolute value of this value needs to be added to the default Temp. Upper Limit (0x04).
4. Another negative offset value example.

Table 3 System Area Memory unlocking and programming

RS485 Page [dec]	RS485 Address [dec]	RS485 Address [hex]	Temperature Sensor Bit 7	6	5	4	3	2	1	0	Default [hex]
9	0	0x00	Unlock System Memory Level 1(Write data 0xAB)								0x00
	1	0x01	Page Program of System Memory (Write data 0xC0)								0x00

NOTE

1. Trigger the Unlock System Memory command when changes to the Level 1 memory is needed.
2. After the change is done at each system memory page, e.g. at Page 7, a Page Program command is needed to store the memory into the internal EEPROM. Allow a delay of minimally 320ms for the page program to complete.
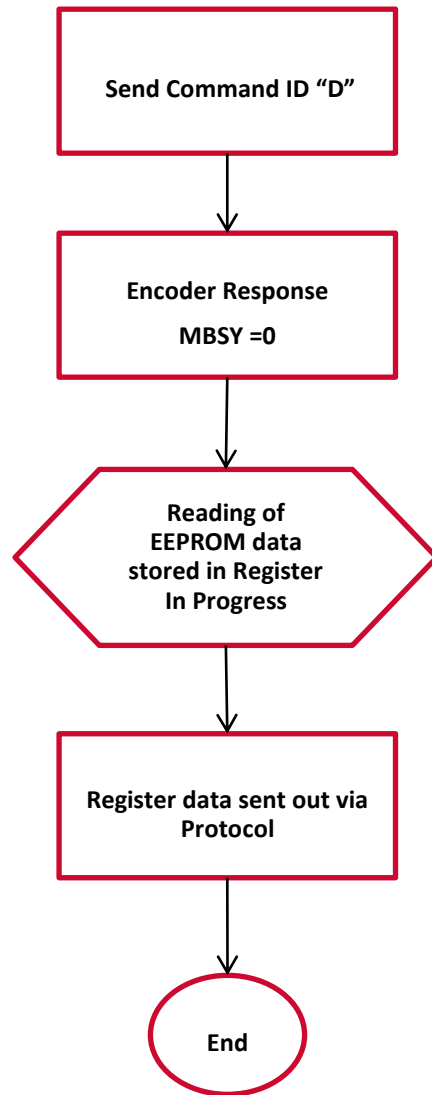
EEPROM User Accessible Memory Area

Table 4 User Accessible Memory Area

Page [decimal]	Address [hex]	Remarks
0 to 4	0x00~0x7E	User Area
Page Selection	0x7F	
11 to 13	0x00~0x7E	
Page Selection	0x7F	

NOTE

1. Total *8* pages with 127 addresses each are allocated for user access.
2. All User accessible addresses are pre-programed to "00" prior to shipment.
3. The active page numbers are specified in address 0x7F, page change is done by writing to address 0x7F. Default Page after power on is Page 0.
4. Once the page value is changed, allow a time delay of 18ms.
5. Typical EEPROM read time is 200µs minimum.
6. Typical EEPROM write time is 6ms minimum.
7. Permissible USER EEPROM writing cycle is 1,000,000 times.
8. Please refer to Appendix A & B for further details on EEPROM Read/Write procedures.

Appendix A

```
┌─────────────────────────┐
│   Send Command ID "D"   │
└─────────────────────────┘
            │
            ▼
┌─────────────────────────┐
│    Encoder Response     │
│        MBSY =0          │
└─────────────────────────┘
            │
            ▼
      ⬡ Reading of ⬡
      EEPROM data
      stored in Register
      In Progress
            │
            ▼
┌─────────────────────────┐
│ Register data sent out  │
│      via Protocol       │
└─────────────────────────┘
            │
            ▼
         ( End )
```

NOTE

1. Each EEPROM reading requires sending a Command ID "D" from the Host.
2. A Command ID "D" from Host will initiate reading Data from Register, MBSY flag will return value "0".

Appendix B
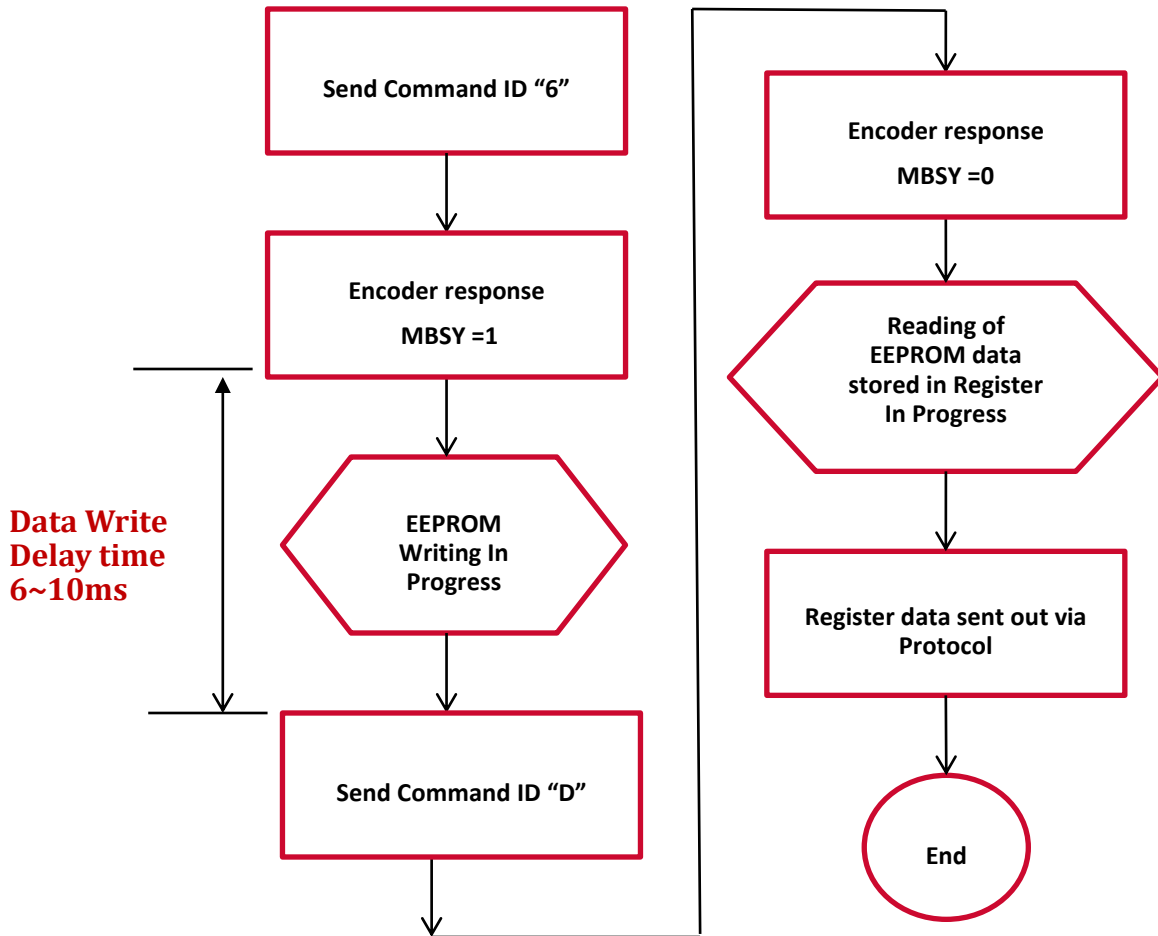
NOTE

1. Every time when issuing of Command ID 6 request, the MDF content writing may not be confirmed even though the MBSY flag returns a value of "0".
2. It is recommended to issue a Command ID "D" request , 6~10ms after the issuance of EEPROM write request to read the designate MDF data for confirmation if the correct data has been successfully written.
3. Encoder will respond with an MBSY status of "1" if the MDF data is written into the external EEPROM (Page 0 to Page 4, and Page 11 to Page 13) with a Command ID 6.
4. Encoder will respond with an MBSY status of "0" if the MDF data is written into the internal register and EEPROM (Page 5 to Page 10) with a Command ID 6.
5. Encoder will respond with an MBSY status of "1" if a page change request (address 0x7F with data value of 0x00 to 0x08, and 0x0B to 0x0D) is sent through a Command ID 6.